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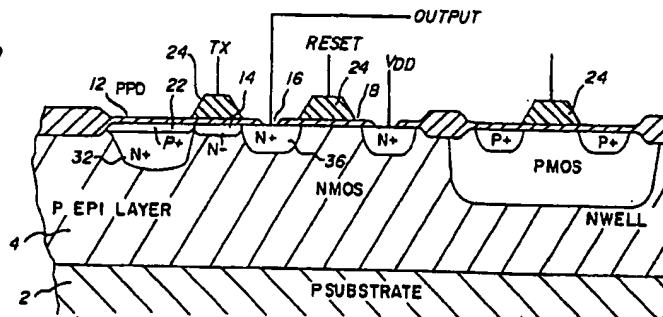
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(54) Active pixel sensor integrated with a pinned photodiode

(57) The optimization of two technologies (CMOS and CCD) wherein a pinned photodiode is integrated into the image sensing element of an active pixel sensor. Pinned photodiodes are fabricated with CCD process steps into the active pixel architecture. Charge integrated within the active pixel pinned photodiode is

transferred into the charge sensing node by a transfer gate. The floating diffusion is coupled CMOS circuitry that can provide the addressing capabilities of individual pixels. Alternatively, a buried channel photocapacitor can be used in place of the pinned photodiode.

FIG. 2



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EP 0 738 010 A2

Description

FIELD OF THE INVENTION

The present invention relates to image sensing devices, and more particularly, to the integration of charge coupled device (CCD) technology within CMOS technology.

BACKGROUND OF THE INVENTION

Active pixel sensors refer to electronic image sensors within active devices, such as transistors, that are associated with each pixel. An active pixel sensor has the advantage of being able to easily incorporate signal processing and decision making circuitry on the same chip. Conventional active pixel sensors typically employ polysilicon photocapacitors or photogates as the active image sensing elements. These conventional active pixel sensors suffer from poor blue color response, high dark current and image lag.

Pinned photodiodes have been employed within charge coupled devices and have shown advantages in the area of color response for blue light, dark current density and image lag. For this reason pinned photodiodes are normally associated with high performance image sensors. Heretofore, pinned photodiodes have typically been employed as photoelements for charge coupled devices. An example of such a use of a pinned photodiode can be seen in THE PINNED PHOTODIODE FOR AN INTERLINE-TRANSFER CCD IMAGE SENSOR, by Burkey et al., IEDM 84, 1984, pages 28-31. However, charge coupled device technology lacks in the amount and type of circuitry elements that can be placed on a device.

From the foregoing discussion it should be apparent that there remains a need within the art of semiconductors for a pinned photodiode employed within a semiconductor technology that can provide advanced circuitry elements.

SUMMARY OF THE INVENTION

The present invention overcomes the shortcomings of the prior art by providing for the optimization of two technologies (CMOS and CCD) wherein a pinned photodiode is integrated into the image sensing element of an active pixel sensor. Pinned photodiodes are normally fabricated with CCD technology. By incorporating the appropriate process steps from CCD technology, a pinned photodiode can be integrated into the active pixel architecture. To improve the blue response and the dark current limitations of the active pixel sensor, a new CMOS imager has been integrated with a pinned photodiode using a mixed process technology. This technology combines CMOS and CCD processes to provide the best features from both technologies.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic diagram of the pinned photodiode based active pixel sensor of the present invention.

FIG. 2 is a cross sectional diagram of the devices used in creating the sensor of the present invention.

FIG. 3a through FIG. 3g illustrate the various process steps employed in creating the device of FIG. 2.

DESCRIPTION OF THE PREFERRED EMBODIMENT

It has been discovered that technological features of a charge coupled device (CCD) can be employed to CMOS type semiconductors to create an active pixel sensor having a pinned photodiode using both technologies.

FIG. 1 shows a schematic diagram of the pinned photodiode based active pixel sensor of the present invention, as employed within a CMOS based signal processing system. To improve the blue response, reduce lag and minimize the dark current characteristics of the active pixel sensor, a new CMOS imager has been integrated with a pinned photodiode 12 using a mixed process technology. This combines n-well CMOS technology and a pinned photodiode CCD processes to provide a sensor having the best features from both technologies. An $n \times m$ pinned photodiode active pixel sensor can be designed and fabricated, where n and m are number of pixels on the edges of the sensor. The present invention has advantages by incorporating image-sensor CCD technology in CMOS active sensor.

FIG. 2 illustrates a cross sectional diagram of the devices used in creating the sensor of the present invention. This is the result of integration of an active pixel sensor (APS) architecture typically fabricated in Complementary Metal Oxide Semiconductor (CMOS) technology with a pinned photodiode 12 (PPD) device using a mixed process technology. This new technology allows mixing of CMOS and high performance Charge-Coupled Device (CCD) modules. The PPD 12 becomes the photoactive element in an XY-addressable area array with each pixel containing active devices for the transfer 14, readout via floating diffusion 16, and reset 18 functions. An n-well CMOS technology was combined with the CCD process to provide the best features from both technologies. By replacing the polysilicon photocapacitor or photogate in conventional APS with the pinned photodiode 12, deficiencies in poor blue response, image lag and high dark current are minimized.

A buried-channel photocapacitor (not shown) biased in the accumulation mode would not have the limitations in dark current that CMOS technology has. A buried channel photocapacitor has essentially equivalent dark current characteristics to the PPD. The blue response problem can also be eliminated by using transparent gating material. An example of such a material would be Indium Tin Oxide (ITO). Therefore, employing both a buried channel photocapacitor with a

transparent gate electrode provides for superior characteristics for blue light response and dark current, similar to those achieved by the PPD. Both the buried channel photocapacitor with a transparent gate and the PPD are devices typically associated with CCD technology. The present invention incorporates these devices from the CCD technology with CMOS processing capabilities. The construction of a active pixel sensor employing a buried channel photocapacitor would be similar to the PPD in FIG. 2 with the photocapacitor structured much like the transfer gate of the PPD embodiment. The transfer gate of the photocapacitor embodiment then would be without the buried channel of the transfer gate used by the PPD embodiment.

The process integration mixes the two technologies resulting in performance which is comparable to that obtained by each of the conventional processes, individually. This was demonstrated on linear image sensors and CMOS test circuits.

In the mixed process technology, schematic representation of the process flow is given in FIG. 3a through 3g.

FIG. 3a illustrates the patterning and ion implantation used within the present invention to form n-well 40 which is used to contain the PMOS transistors that will form part of the control circuits of present invention.

FIG. 3b and 3c show the patterning and growth of isolation oxide/field oxide which is used for isolating devices to be formed on the silicon layer 2 with or without epitaxial layers and with or without wells structures.

FIG. 3d illustrates the patterning and ion implantation of an n-type buried channel 15 which is used to form the transfer gate 14 of the pixel within the present invention. After the implantation of the buried channel 15, photoresist layer 52 is removed and a polysilicon layer 26 is formed upon the substrate. The polysilicon 26 is used to form local interconnects and the gates of transistors. Both PMOS and NMOS transistors will have their gates formed by this polysilicon 26.

FIG. 3e shows the patterning of the polysilicon 26 with photoresist 54 and implantation of N⁺ dopant to form source and drain regions. This results in source and drain regions that are self aligned to the remaining polysilicon 26. This forms the NMOS transistors within the preferred embodiment.

FIG. 3f show the construction of the PPD by patterning with photoresist 56 areas for two additional implants. The first implant is to create a photodiode by implanting a deeper N⁺ impurity than was previously used by the source and drain implants discussed above. The deeper implant yields substantial increases in photo response due to an increase collection path for the incident photo carriers with the deeper implant. A pinning layer 22 implant is then made using high doses of low energy P⁺ dopant that remains near the surface of the photodiode 32.

FIG. 3g shows the patterning with photoresist 58 and the following ion implantation of the source/drains of the PMOS transistors. As with the NMOS transistors,

the source/drain implants for the PMOS transistors are self aligned with the selected polysilicon. P⁺ implant are used to construct the PMOS transistors.

The device is completed by the appropriate planarization and metalization steps.

The imager architecture of the present invention can be employed to signal processing circuitry of prior art devices to increase their overall performance. An example is the incorporation of the present invention into an earlier designs implemented at Jet Propulsion Laboratory. This earlier design is described in IEEE Transactions on Electron Devices, Vol. 41, No. 3, March 1994 (hereinafter referred to as JPL). While describing a photogate integrated into an active pixel sensor, the device as taught by JPL did not provide a sensor that yielded satisfactory blue wavelength color response. Additionally, the JPL device lacked sufficient low dark current noise characteristics. The present invention overcomes these shortcomings by incorporating pinned photodiode technology not conventionally applied within CMOS technology. This results in an image sensor having superior response for blue light and improved dark current noise characteristics.

While the best mode known to the inventor has been disclosed by the preferred embodiment, various modifications will be obvious to those skilled in the art. These obvious modifications should be considered in view of the appended claims.

Claims

1. A method for integrating a pinned photodiode into an active pixel sensor comprising the steps of:

providing a substrate made from a semiconductor material of a first conductivity type with a series of masking layers including at least one conductive layer on a major surface of the substrate;
forming at least one well of a second conductivity type that is opposite the first conductivity type in area where control circuitry is to be built, and forming an active area over the substrate;
patterning at least one transfer gate and a series of local interconnections;
forming structures for a charge sensing means, including, creating patterns representing a first set of sources and drains for a predetermined set of transistors, including at least one drain for each of the transfer gates such that the drain is self aligned to the transfer gate;
implanting a second conductivity type opposite the first conductivity type as to create the first set of sources and drains;
patterning at least one image sensing area adjacent to the transfer gate;
implanting within the image sensing area a material of the second conductivity type to create a photodiode;

- implanting on top of the photodiode a pinning layer comprising the first conductivity type;
creating patterns representing a second set of sources and drains for a predetermined set of transistors;
implanting the first conductivity type to create the second set of sources and drains; and
creating a predetermined set of contacts on first and second set of source drains.
2. The method of claim 1 further comprising the step of providing a transfer region of the second conductivity type below the transfer gate such that it is essentially self aligned with the transfer gate side opposite the photodiode.
 3. The invention of claim 2 wherein the step of implanting on top of the photodiode a pinning layer further comprises implanting the first conductivity type such that it has at least one edge that overlaps the transfer region and is at the surface of the second conductivity type.
 4. The invention of claim 1 further comprising the step of providing the drain self aligned to the transfer gate is a floating diffusion region that is coupled to the second set of sources and drains.
 5. The method of claim 1 wherein the steps relating to implanting the first and second sets of sources and drains are reversed.
 6. An active pixel sensor having at least one pinned photodiode comprising:
 - a substrate of a semiconductor material of a first conductivity type having a series of masking layers including at least one conductive layer, and at least one charge sensing means; at least one transfer gate and a series of local interconnections upon the conductive layer;
 - a first set of implants made from a second conductivity type that is opposite the first conductivity type, the first set of implants functioning as sources and drains for a first set of transistors, including at least one source for each of the transfer gates such that the drain is self aligned to the transfer gate;
 - at least one image sensing area adjacent to the transfer gate formed from one of the sources implanted within the substrate to create a photodiode, with a pinning layer comprising a material of the first conductivity type on top of the photodiode;
 - a second set of implants used as sources and drains for a second set of transistors made from implants of the first conductivity type, the second set of transistors being formed in conjunction with any remaining the first set of transistors that were not used to create image sensors to form a CMOS control circuit couple to the image sensor by the local connection; and
 - a predetermined set of contacts on first and second set of source drains.
 7. The pixel sensor of claim 6 further comprising a transfer region of the second conductivity type below the transfer gate such that it is essentially self aligned with the side of the transfer gate adjacent to the photodiode.
 8. The pixel sensor of claim 7 wherein the pinning layer further comprises that it has at least one edge that is self aligned to the side of the transfer region adjacent to the photodiode.
 9. The pixel sensor of claim 6 further comprising the charge sensing means is a drain being self aligned to the transfer gate comprising a floating diffusion region that is coupled to the second set of sources and drains.
 10. The pixel sensor of claim 6 wherein the image sensing area is an array of pinned photodiodes that is operatively controlled by the CMOS control circuit via the local interconnections.

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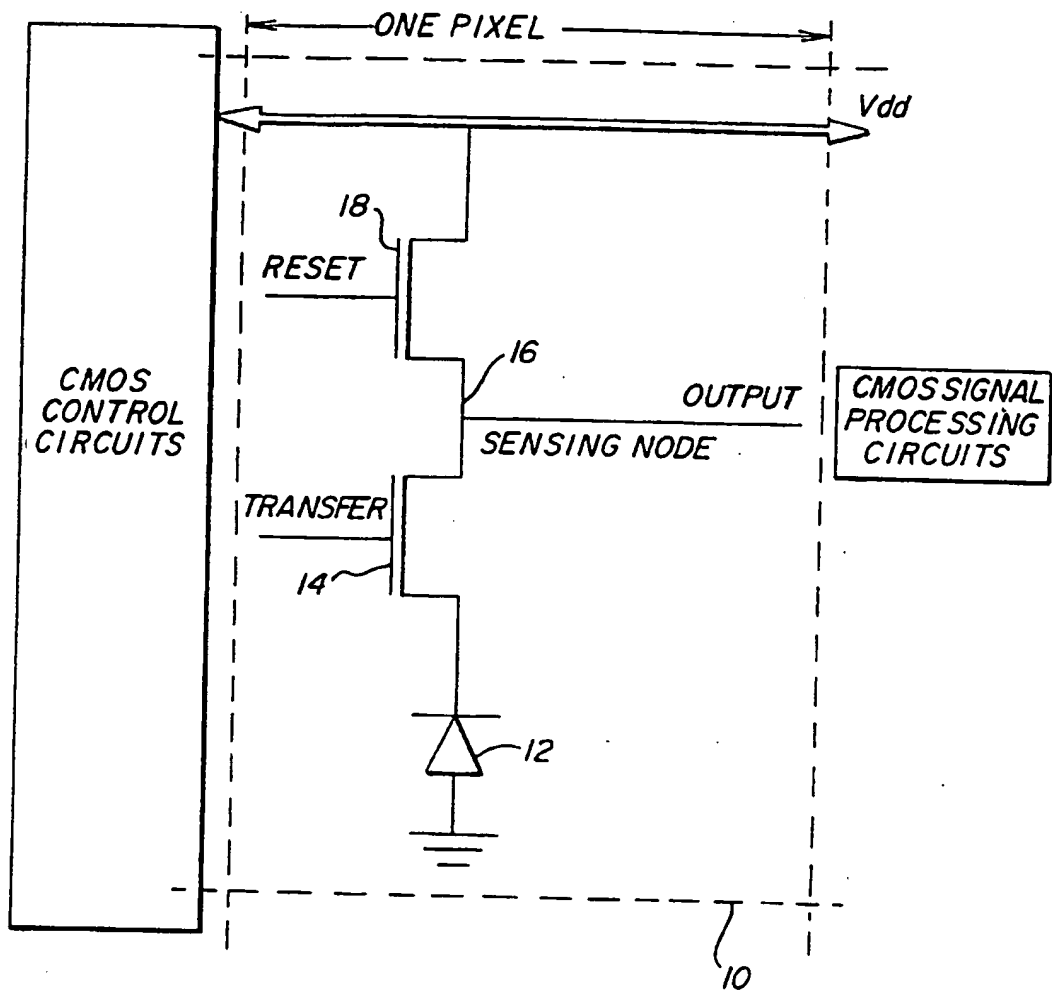


FIG. 1

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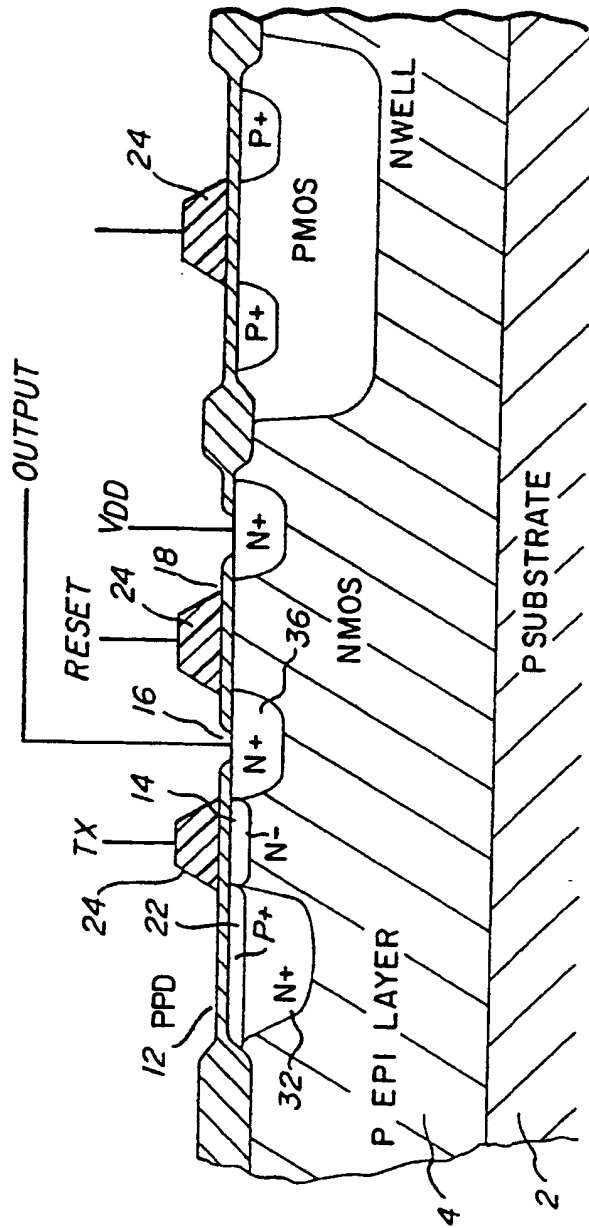


FIG. 2

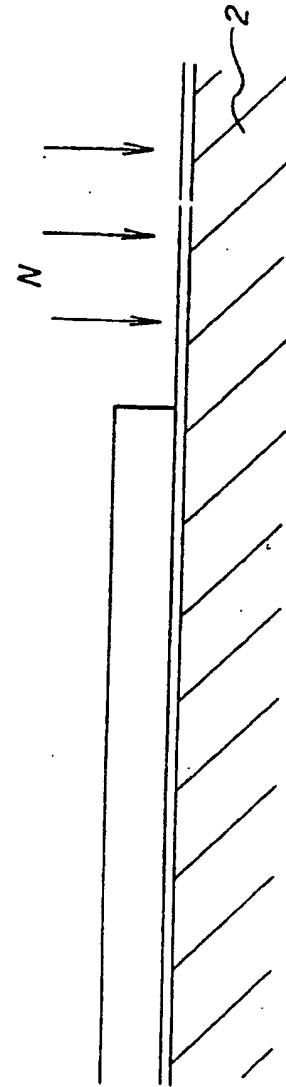


FIG. 3(a)

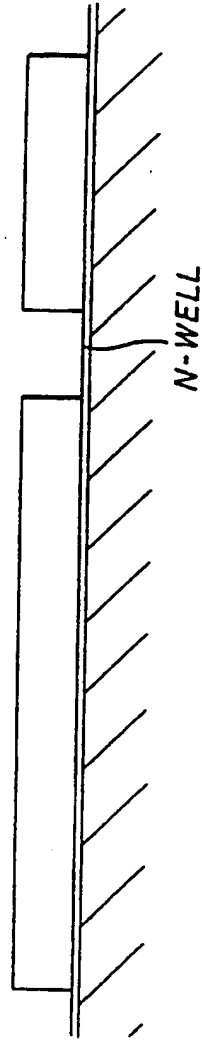


FIG. 3(b)

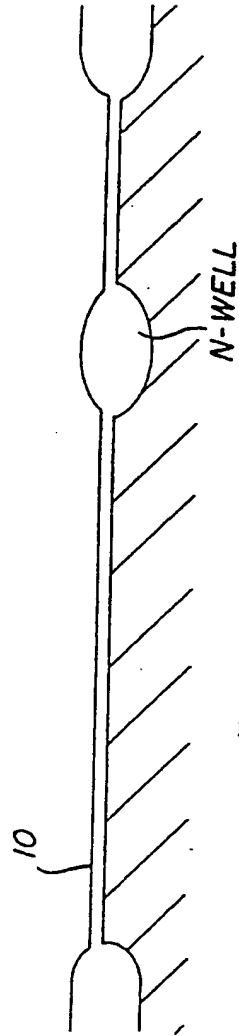


FIG. 3(c)

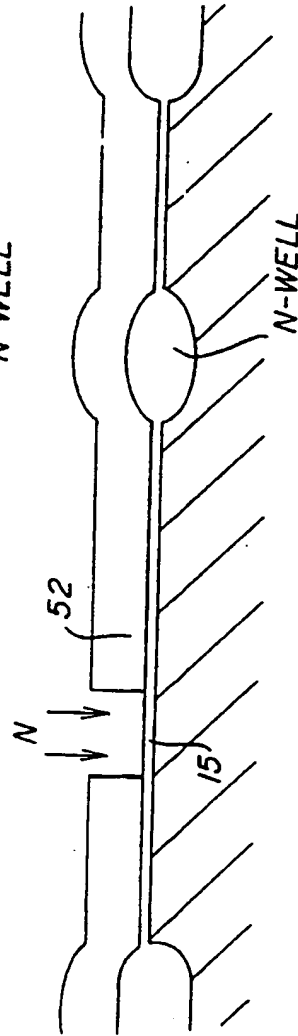


FIG. 3(d)

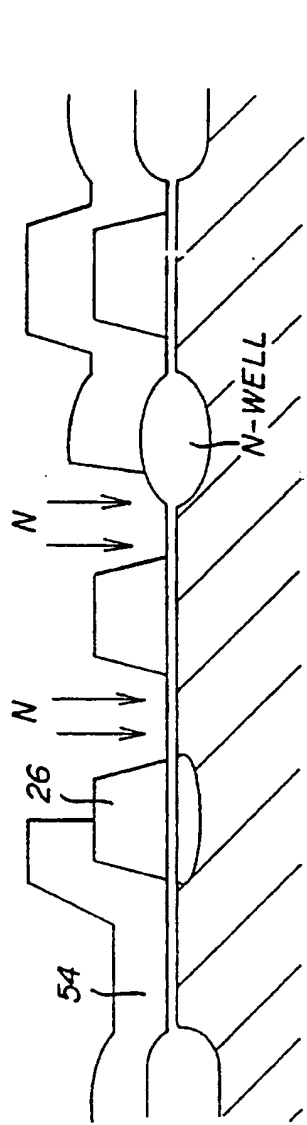


FIG. 3(e)

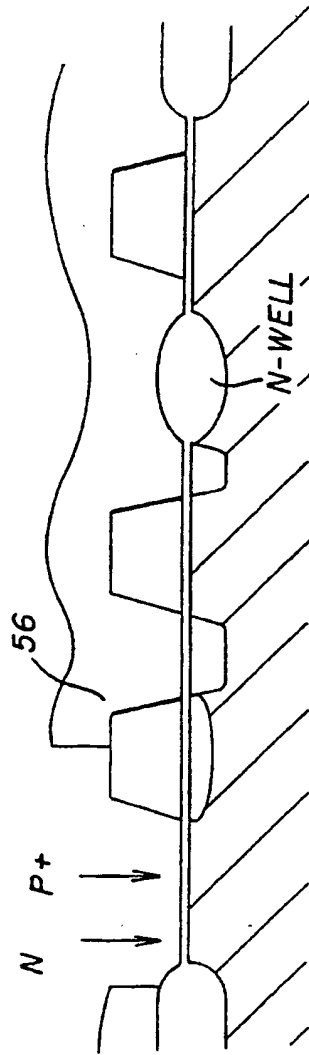


FIG. 3(f)

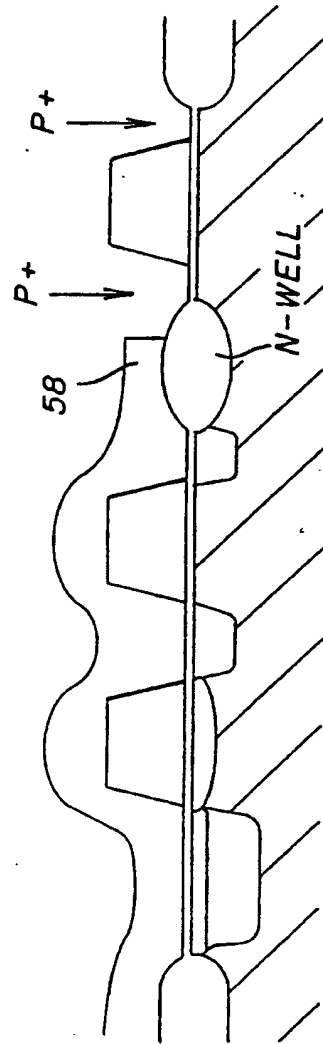


FIG. 3(g)

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